WHAT IS CLAIMED IS:

1. A manufacturing method of a thin film transistor (TFT), comprising:

forming a gate over a substrate;

forming an inter-gate dielectric layer over the substrate covering the gate;

forming a channel layer over a portion of the inter-gate dielectric layer at least over the gate, wherein the channel layer comprises a lightly doped amorphous silicon layer; and

forming a source/drain regions over the channel layer, wherein the source/drain regions are separated by a distance.

2. The manufacturing method of claim 1, wherein the channel layer comprises an N-type lightly doped amorphous silicon layer.

3. The manufacturing method of claim 1, wherein the channel layer comprises a P-type lightly doped amorphous silicon layer.

4. The manufacturing method of claim 1, wherein the channel layer is doped with phosphorous atoms, and a concentration of phosphorous atoms is in a range of about 1E17atom/cm^3 to about 1E18atom/cm^3.

5. The manufacturing method of claim 1, wherein the channel layer is doped with boron atoms, and a concentration of boron atoms is in a range of about 1E16atom/cm^3 to about 5E17 atom/cm^3.

6. The manufacturing method of claim 1, wherein the step of forming the channel layer comprises performing a chemical vapor deposition (CVD) process using a reaction gas mixture comprising silane (SiH_4), hydrogen and phosphine (PH_3), wherein a flow ratio of the phosphine (PH_3) is in a range of about 0.28ppm to about 8ppm, and

wherein the flow ratio of the phosphine (PH_3) is equal to the ratio of the flow of phosphine (PH_3) to the total flow of silane (SiH_4), hydrogen and phosphine (PH_3).

7. The manufacturing method of claim 1, wherein the step of forming the channel layer comprises performing a chemical vapor deposition (CVD) process using a reaction gas mixture comprising silane (SiH_4), hydrogen and boroethane (B_2H_6), wherein a flow ratio of the boroethane (B_2H_6) is in a range of about 0.5ppm to about 10ppm, and wherein the flow ratio of the boroethane (B_2H_6) is equal to the ratio of the flow of boroethane (B_2H_6) to the total flow of silane (SiH_4), hydrogen and boroethane (B_2H_6).

8. The manufacturing method of claim 1, wherein the step of forming the channel layer comprises:

forming a first lightly doped amorphous silicon layer over the portion of the inter-gate dielectric layer at a first deposition rate; and

forming a second lightly doped amorphous silicon layer over the first lightly doped amorphous silicon layer at a second deposition rate, wherein the first deposition rate is lower than the second deposition rate.

9. The manufacturing method of claim 1, further comprising a step of forming an ohmic contact layer over the channel layer between the step of forming the channel layer and the step of forming the source/drain regions.

10. The manufacturing method of claim 1, further comprising a step of forming a protection layer over the substrate after the step of forming the source/drain regions covering the source/drain regions, the channel layer and the inter-gate dielectric layer.

11. A thin film transistor (TFT), comprising:

a substrate;

a gate, disposed over the substrate;

an inter-gate dielectric layer, disposed over the substrate covering the gate;

a channel layer, disposed over a portion of the inter-gate dielectric layer, at least over the gate, wherein the channel layer comprises a lightly doped amorphous silicon layer; and

a source/drain regions, disposed over the channel layer, wherein the source/drain regions are separated by a distance.

12. The thin film transistor (TFT) of claim 11, wherein the channel layer comprises an N-type lightly doped amorphous silicon layer.

13. The thin film transistor (TFT) of claim 11, wherein the channel layer comprises a P-type lightly doped amorphous silicon layer.

14. The thin film transistor (TFT) of claim 11, wherein the channel layer is doped with phosphorous atoms, and a concentration of phosphorous atoms is in a range of about 1E17atom/cm^3 to about 1E18atom/cm^3.

15. The thin film transistor (TFT) of claim 11, wherein the channel layer is doped with boron atoms, and a concentration of boron atoms is in a range of about 1E16atom/cm^3 to about 5E17atom/cm^3.

16. The thin film transistor (TFT) of claim 11, wherein the channel layer comprises:

a first lightly doped amorphous silicon layer, disposed over a portion of the inter-gate dielectric layer; and

a second lightly doped amorphous silicon layer, disposed over the first lightly doped amorphous silicon layer.

17. The thin film transistor (TFT) of claim 11, further comprising an ohmic contact layer between the channel layer and the source/drain regions.

18. The thin film transistor (TFT) of claim 11, further comprising a protection layer over the substrate, wherein the protection layer covers the source/drain regions, the channel layer and the inter-gate dielectric layer.